ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, $VDRV_{CC}$ = $VINTV_{CC}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator							
V_{IN}	Input Supply Voltage		●	4.5		35	V
I_Q	Input Quiescent Current, I_{VOUT} (Note 4)				2.25		mA
$V_{CAPFBHI}$	Maximum Regulated V_{CAP} Feedback Voltage	Full Scale (1111b)	●	1.188	1.2	1.212	V
V_{CAPFB_DEF}	Default V_{CAPFB_DAC} Setting	(1010b)	●	0.997	1.0125	1.028	V
$V_{CAPFBLO}$	Minimum Regulated V_{CAP} Feedback Voltage	Zero Scale (0000b)	●	0.625	0.6375	0.650	V
I_{CAPFB}	CAPFB Input Leakage Current	V_{CAPFB} = 1.2V	●	–50		50	nA
V_{OUTFB}	Regulated V_{OUT} Feedback Voltage		●	1.182	1.2	1.218	V
$V_{OUTFB(TH)}$	OUTFET Turn-Off Threshold	Falling Threshold		1.27	1.3	1.33	V
I_{OUTFB}	OUTFB Input Leakage Current	V_{OUTFB} = 1.2V	●	–50		50	nA
V_{OUTBST}	V_{OUT} Voltage in Step-Up Mode	V_{IN} = 0V	●	4.5		35	V
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.85	4.3 4	4.45	V V
$V_{DRVUVLO}$	DRV_{CC} Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.75	4.2 3.9	4.35	V V
V_{DUVLO}	V_{OUT} – V_{CAP} Differential Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	160 55	200 90	240 125	mV mV
V_{OVLO}	Switcher V_{IN} Overvoltage Lockout	Rising Threshold Falling Threshold	● ●	37.7 36.3	38.6 37.2	39.5 38.1	V V
V_{VCAPP5}	Charge Pump Output Voltage	Relative to VCAP, 0V < V_{CAP} < 20V			5		V
Input Current Sense Amplifier							
V_{SNSI}	Regulated Input Current Sense Voltage (ISNSP_CHG – ISNSM)		●	31.04	32	32.96	mV
Charge Current Sense Amplifier							
V_{SNSC}	Regulated Charge Current Sense Voltage (I_{CAP} – V_{CAP})	V_{CAP} = 10V, Charge Mode	●	31.04	32	32.96	mV
V_{CMC}	Common Mode Range (ICAP, VCAP)			0		20	V
V_{PEAK}	Peak Inductor Current Sense Voltage	Active in Both Step-Up/Step-Down Modes	●	51	58	65	mV
I_{ICAP}	ICAP Pin Current	Step-Down Mode, VSNSC = 32mV Step-Up Mode, VSNSC = 32mV			27 100		µA µA
Error Amplifier							
g_{MV}	V_{CAP} Voltage Loop Transconductance				1		mmho
g_{MC}	Charge Current Loop Transconductance				64		µmho
g_{MI}	Input Current Loop Transconductance				64		µmho
g_{MO}	V_{OUT} Voltage Loop Transconductance				350		µmho
Oscillator							
f_{SW}	Switching Frequency	RT = 107k	●	493	500	507	kHz
	Maximum Programmable Frequency	RT = 53.6k			1		MHz
	Minimum Programmable Frequency	RT = 267k			200		kHz
DCMAX	Maximum Duty Cycle	Step-Down Mode, 53.6k < R_T < 267k Step-Up Mode, 53.6k < R_T < 267k		97 87	98 93	99.5	% %

replace with below spec

f_{SW}	Switching Frequency	R_T = 107k	 ●	495 490	500 500	505 510	kHz kHz

3351f

APPLICATIONS INFORMATION

Hot Swap Component Selection

The hot swap controller will servo the HS_GATE pin to regulate the voltage across the sense resistor(s) between ISNSP_HS and ISNSM to be, at most, 48mV ($V_{ILIM(TH)}$) . This current limit is folded back as the voltage between V_{IN} and V_{OUT} increases to 12V, at which point the regulation voltage drops to 12mV and no further.

The CSS capacitor is used both to set an input qualification delay (debounce) and to limit the V_{OUT} dV/dt rate to limit the inrush current.

$$dV_{OUT}/dt = 48\mu A/C_{SS}$$

$$t_{DELAY} = \frac{1.2V \bullet C_{SS}}{1\mu A}$$

The primary concern when selecting a CSS capacitor value is to select a value large enough to slow the V_{OUT} rise rate such that the input current stays below the minimum hot swap current limit due to foldback. The following equations are for input voltages above 10V and assume a 12mV minimum current limit voltage. The minimum C_{SS} capacitor could be reduced further for lower voltage inputs due to the minimum current limit voltage being higher due to less foldback. The following equations assume any V_{OUT} load remain off until after the hot swap completes, if loads are present on VOUT the CSS capacitor must be further ~~reduced~~ increased to set a V_{OUT} rise rate such that the dV/dt • C_{OUT} current and the load current do not exceed the folded back current limit at any point.

The maximum dV/dt of the output without reaching current limit is

$$\frac{dV_{OUT}}{dt} = \frac{12mV}{R_{SNS} \bullet C_{OUT}}$$

$$\text{Minimum } C_{SS} = \frac{48\mu A}{12mV} \bullet R_{SNS} \bullet C_{OUT} = 4mmho \bullet R_{SNS} \bullet C_{OUT}$$

The C_{SS} capacitance may be increased to any value to achieve a longer delay, however it must be larger than the minimum C_{SS} computed above to avoid current limit and tripping the circuit breaker.

The switcher and hot swap controller both share the negative terminal for their current sense amplifiers. The switcher reduces charger current so that there is at most 32mV between ISNSP_CHG and ISNSM and the hot swap controller will limit the input current to at most 48mV between ISNSP_HS and ISNSM. This allows a single sense resistor to be used in many applications, resulting in a hot swap circuit breaker that is 50% higher than the switcher's input current limit. Any two values may be selected by using two current sense resistors, see the Input Sense Resistors Selection section of this data sheet for more information.

Setting Switcher Input and Charge Currents

The maximum switcher input current is determined by the resistance across the ISNSP_CHG and ISNSM pins, typically R_{SNSI}. The maximum charge current is determined by the value of the sense resistor, R_{SNSC}, connected in series with the inductor. The input and charge current loops servo the voltage across their respective sense resistor to 32mV. Therefore, the maximum input and charge currents are:

$$I_{IN(MAX)} = \frac{32mV}{R_{SNSI}}$$

$$I_{CHG(MAX)} = \frac{32mV}{R_{SNSC}}$$

The peak inductor current limit for both buck and boost modes, I_{PEAK}, is 80% higher than the maximum charge current and is equal to:

$$I_{PEAK} = \frac{58mV}{R_{SNSC}}$$

This current limit is active in both charging and backup modes. In backup mode, it is the only control limitation on inductor and output current.

Low Current Charging and High Current Backup

The LTC3351 accommodates applications requiring low charge currents and high backup currents. In these applications, program the desired charge current using R_{SNSI}. The higher current needed during backup is set using R_{SNSC}. The input current limit will override the charge current